# Scaling and materials effects on CPI failure and potential solutions

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## Introduction

The introduction of low-k and ultra low-k dielectric constant materials has had a significant adverse effect on the mechanical integrity of semiconductor devices. As the dielectric constant is reduced, so are the mechanical properties of the dielectrics and the interfaces they form. The result of these reduced properties is manifested in delaminations which propagate from the mechanically diced edge of the silicon die, through the crackstop or guard-ring and into the active portion of the device causing failure. These delaminations are driven by the thermal mismatch between the die and the packaging material which encapsulates the chip. These delaminations often occur during chip-package stresses which typically range from -55°C to 125 °C for several hundred or one thousand cycles. This paper seeks to highlight some of the trends associated with scaling both in terms of lower dielectric constant and feature size. In addition this paper will also highlight some of the key elements associated with the energy supplied by the package which causes delamination. Finally, potential methods for preventing or stopping delaminations are discussed.

## Experimental

Quantitative adhesion measurements were made using standard sandwiched four-point flexure fracture mechanics specimens as described in previous publications. [1] Interfacial debond energies were calculated from the data. The reported results were averaged over measurements from six to ten samples with the error reported representing one standard deviation.

## Scaling and materials trends

Average cohesive strength values for a range of Si based dielectrics as determined by four point flexure samples are shown in Figure 1. [2] The data show a linear decrease in cohesive strength with dielectric constant dropping from ~10 $J/m^2$ for $SiO_2$ to approximately 3 $J/m^2$ for a dielectric constant of 2.2. This trend is consistent with the Si-O bond density being responsible for both the cohesive strength and the majority of the dielectric constant. In the absence of secondary energy absorbing processes, the cohesive strength provides an upper bound for the adhesive strength of the dielectric. However, careful consideration must be given to the interfacial treatment to insure that maximum values are achieved for the adhesion of the dielectric. Table I gives values of adhesion for several PECVD Si-based dielectrics deposited on a SiCNH film with different substrate treatments. [3] The substrate treatments include no initial treatment, an initial oxidation of the SiCNH and an oxide transition layer between the SiCNH film and the dielectric.

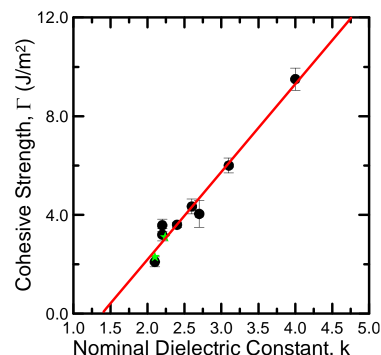



**Figure 1:** Cohesive strength values for a range of Si-O based dielectrics. [2]

**Table I: Improvement of interfacial strength to SiCNH for different SiCOH films [3]**

| SiCOH version | Bulk-only SiCOH ($J/m^2$) | Substrate treatment ($J/m^2$) | Optimized transition ($J/m^2$) | Cohesive strength ($J/m^2$) |
|---|---|---|---|---|
| k=3.0 | 2.0 (0.1) | 3.0-4.0 (0.2) | 5.0 (0.2) | 6.0 (0.3) |
| k=2.7 | 2.0 (0.1) | N/A | 4.5 (0.2) | 5.3 (0.3) |
| k=2.4 | 2.0 (0.1) | N/A | 3.5 (0.3) | 3.5 (0.2) |

The utilization of the optimized adhesion layer brings the adhesive strength close to that of the cohesive strength of the dielectric. Failure to do so can lead to increased failures of the type shown in Figure 2 where delaminations generated during mechanical dicing propagate through the crackstop whose purpose is to protect the active part of the die from outside defects.

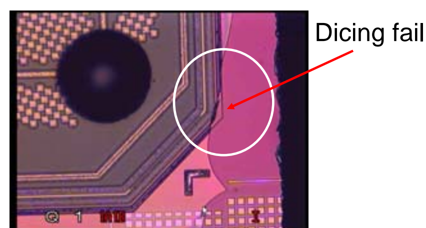



**Figure 2:** A delamination that has penetrated the crackstop and into the active part of the die resulting in a failure.

Table I and Figures 1 and 2 highlight the difficulties faced in continually reducing the dielectric constant. As the dielectric constant is reduced the maximum attainable adhesive strength will decrease accordingly. As the adhesion strength decreases, the susceptibility to failures like those shown in Figure 2 increases. However, the dielectric ad-

hesion to a SiCNH film is not the only concern as the technology scales. As the critical feature size is decreased with each new generation, the crackstop toughness is expected to decrease as well. In general, the crackstop has a form similar to that shown in Figure 3 where two metal plates or pads are connected by metal vias or bars.

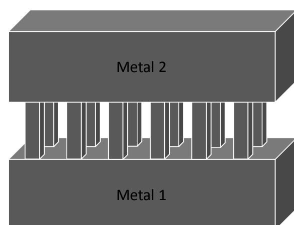



**Figure 3:** A schematic cross-section of a typical crackstop structure where metal plates are connected by metal vias, and the crackstop is a monolithic structure separating the active die from the die edges.

Recent work has focused on optimizing the via structure which connects the plates with impressive increases in crackstop toughness. [4] However, even though the via structure may be optimized the crackstop structure is expected to decrease in toughness with scaling due to effects similar to that shown in Figure 4. [5]

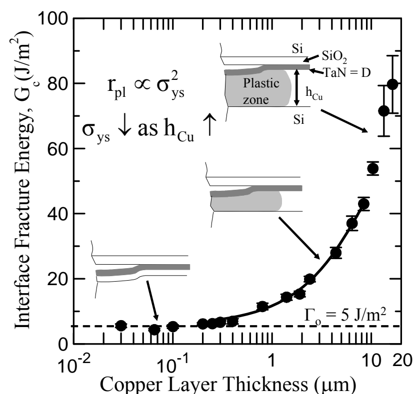
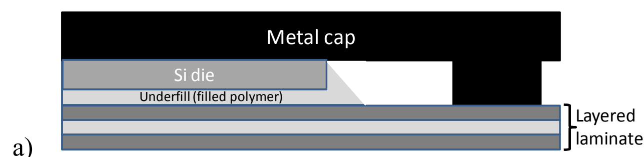



**Figure 4:** Interface fracture energy of a TaN/$SiO_2$ interface with varying thicknesses of Cu next to the TaN layer. [5]

As the Cu layer thickness is decreased the toughness decreases due to a loss of plasticity in the ductile Cu layer. The loss of toughness due to decreased metal layer thickness will place increased emphasis on interfacial adhesion optimization to prevent failures such as those in Figure 2.

Not all failures occur during dicing however. Many defects occur during die-wafer separation and then propagate when placed in a package such as that shown in Figure 5a. The thermal mismatch between the plastic package and the die result in an applied strain energy release rate vs. a delamination length curve such as that shown in Figure 5b.

a)




b)

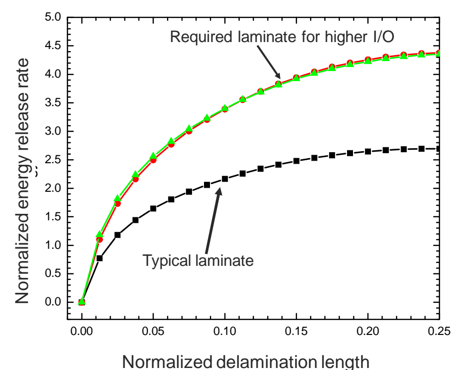


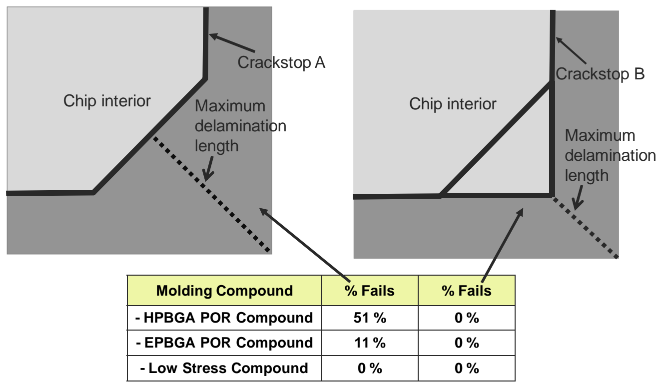

**Figure 5:** a) A typical packaged die. b) Energy release rate vs delamination length for the type of package shown in Figure 5a [6].

Figure 5b indicates that even small flaws initiated during dicing that do not reach the crackstop may propagate and cause failure of the crackstop during thermal cycling. Figure 5b also shows the trend expected with new generations of semiconductor devices. As the requirement for higher I-O densities continues to rise, the energy supplied by the package to the die will increase as the laminate thickness increases. [6] This will increase the requirements on interfacial adhesion and crackstop toughness.

Each of the material and size scaling trends have indicated a negative impact on the robustness of the die. The adhesion of the dielectric layer is expected to decrease with each new generation as is the crackstop toughness. At the same time, the increase in I-O requirements results in thicker laminates which place higher driving energies on the interfaces and makes delamination growth more likely. However, the trend in energy release rate with delamination length shown in Figure 5b indicates potential paths to preventing delaminations as will be discussed in the next section.

## Potential solutions

Figure 5b indicates that the energy supplied by the package to the back-end of the line is strongly dependent on the size of the delamination. Accordingly, if the delamination size can be kept small, failures can be avoided because the applied strain energy release rate is kept below the interfacial strength and/or crackstop toughness. One such example of this is shown in Figure 6 where small changes were made in the crackstop design in order to limit the maximum size of the defect.




| Molding Compound | % Fails | % Fails |
|---|---|---|
| - HPBGA POR Compound | 51 % | 0 % |
| - EPBGA POR Compound | 11 % | 0 % |
| - Low Stress Compound | 0 % | 0 % |

**Figure 6:** The results of a change in crackstop design from one that allowed a large delamination length to one that limited it in size and the resulting fails (penetration of the crackstop) during a thermal cycling test (1000 cycles from -65 to 125 $^{o}$C). [7]

The result in Figure 6 indicates several possibilities to improve the mechanical robustness of microelectronic devices. One possibility is highlighted in Figure 7.

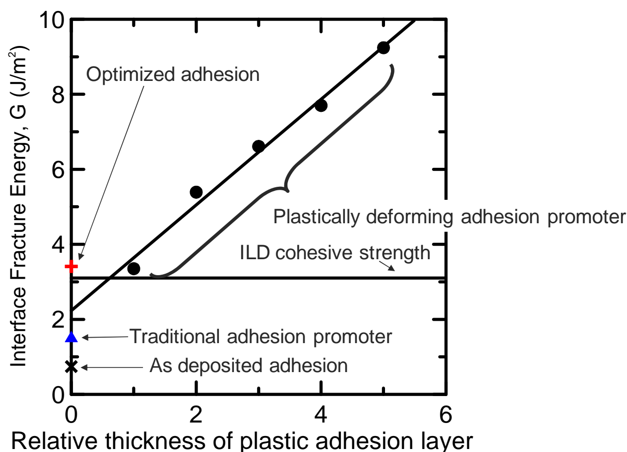



**Figure 7:** The effect of a plastically deforming layer on the interfacial toughness at the ILD/SiCNH interface.

Figure 7 indicates that adding a plastically deforming adhesion layer between the ILD and the SiCNH film can increase the interface fracture energy by ~10x. This effect could be used to limit initial defect sizes during dicing and stop propagation during thermal cycling. The plasticity could potentially be introduced in the dielectric itself eliminating the need for a discrete layer.

A second possible solution avoids the potential complications of introducing a new film that plastically deforms or developing a dielectric that deforms. Here a post-dicing treatment is used to repair delaminations with molecular nanolayers. The concept is shown in Figure 8a. By repairing the interface, the energy supplied by the package to the interface can be limited as shown schematically in Figure 8b.

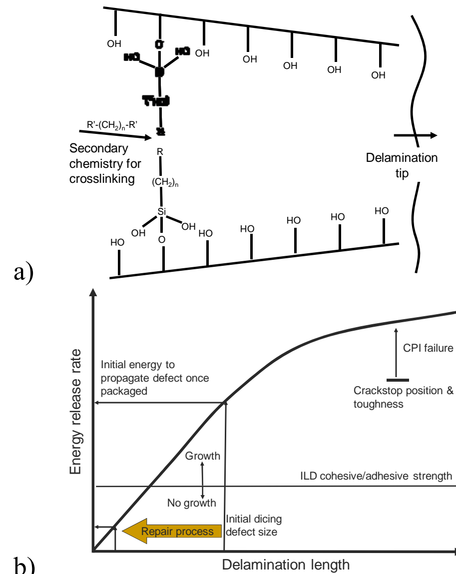



**Figure 8:** a) Potential molecular repair chemistry used to repair delaminations created during dicing. b) Effect of repairing delaminations on applied strain energy release rate.

## Conclusions

Scaling trends in lower dielectric constant materials, smaller feature size and increased package laminate thickness indicate a greater probability of interfacial delamination during die dicing and chip-package thermal cycling. Optimization of crackstop structures may improve crackstop toughness but ultimately the toughness is expected to drop due to reduced plasticity. Alternative energy dissipation processes, such as plastic adhesion layers, and post-dicing interfacial repair may ultimately provide long term reliability by limiting defect sizes and energy transferred from the package to the dielectric interfaces.

## References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