

MODELLING SOLDER JOINT RELIABILITY OF BGA PACKAGES SUBJECT TO DROP IMPACT LOADING USING SUBMODELLING

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1. Abstract

With the trend towards miniaturization and multi-functionality in products such as mobile electronic devices, miniature IC packaging such as fine pitch Ball Grid Array (BGA) package and Chip Size Package (CSP) are increasingly being used. However, the inherent vulnerability of these miniature IC packagings has brought along new reliability problems. Among them, the drop/impact robustness is the most challenging in terms of testing and designing. The minute solder interconnections used to attach these packages to the printed wire board (PWB), in particular, are very vulnerable to drop impact loads, which mobile electronic equipment is reasonably expected to experience during usage.

A major challenge facing the IC package supplier is the ability to assess the reliability of the interconnection when assembled into a product that can take many forms and shape. The Joint Electron Device Engineering Council (JEDEC) is proposing a standardised methodology using a board level drop impact test. However, correlation between the board level drop impact test and the actual product drop remains unclear. This can be best understood through modelling and simulation using Finite Element Analysis techniques.

In this paper initial results are presented of work carried out using ABAQUS Finite Element Analysis software to model the board level drop impact test and hence determine the stress and strain state in the solder joint. The modelling work was divided into two stages: Dynamic modelling of the impact of the complete board assembly using beam and shell elements, followed by submodelling of the minute solder joints using solid elements. The model was subsequently validated against a fine mesh full dynamic model, the analysis time for this model was almost two days. The submodel approach allowed a full global and local simulation to be completed in less than 4 hours, all models being analysed on an Intel Pentium 4 at 1.8Ghz.

Due to the substantially reduced runtime of the validated submodel it may be of great benefit for conducting parametric studies that would aid in the design of board level tests that best simulate the drop impact tests. This modelling technique will also accelerate the development of models to simulate drop tests on production components.