Kuan Hsun Lu EM 397 Thin Film Mechanics Case Study Report:

Channel Cracking of Low-k Dielectric Materials in Multilayer Structure

Dec. 18, 2006

Case study report:

Introduction

Today low dielectric materials are integrated into high performance chips to improve performance and reduce cross-talk noise. Due to the weak mechanical properties of low dielectric materials, delaminating or cohesive failure is subjected to occur. Channel cracking is one common mode of cohesive failure. In this case study report, two potential issues relevant to channel cracking of low dielectric thin films are reviewed, and some design rules are also discussed.

Substrate constrain factor

The energy release rate, G, for channel cracking is calculated from the following equation: $G = Z \frac{\sigma^2 h}{\overline{E}}$ (eqn. 1), where h, σ , \overline{E} are the film thickness, stress, and plane-strain elastic modulus. Z is a constant which comes from the constraining between the thin film and the substrate. Z depends on the elastic mismatch and the geometry. Beuth^{*1} solved the factor Z as a function of Dundeurs parameter α (where $\alpha = \frac{\overline{E}_f - \overline{E}_s}{\overline{E}_f + \overline{E}_s}$), and the numerical result is plot in Fig.1:

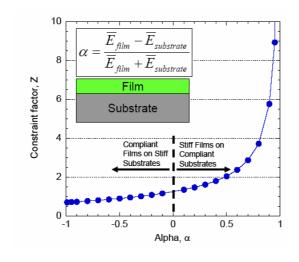


Fig.1: Plot of the constrain factor Z as a function of Dundurs parameter α with β = α /4

From Beuth's calculation we can see: while a compliant film is on a stiff substrate, the driving force of channel cracking is not sensitive to the substrate properties. On the other hand, if a stiff film is on a compliant substrate the driving force would raise up quickly.

Buffer layer effect

Beuth's model is for thin films on a half space substrate. In order to understand the channel cracking in multilevel interconnect structures, Tsui*2 has completed one set of experiment to study the channeling crack behavior of low-k films on top of a bi-layer substrate. Figure 2 shows the scheme of the tested samples, and Table 1 lists the mechanical properties of the materials.

Low-k (CDS)
Low-k (LD-SiCO), polymer
Si substrate

	Elastic modulus (GPa)	Plane-strain modulus (GPa)	Residual stress (MPa)
Si*	163	172	n/a
SiN _x	155	165	-125 <u>+</u> 5
SiO ₂	70	75	-135 <u>+</u> 5
CDS	8.0	8.5	60 <u>+</u> 2
Polymer	3.5	3.7	60 <u>+</u> 2
LD-CDO	3.5	3.7	60 <u>+</u> 3

Fig.2: CDS low-k film on top of a bi-layer substrate

Table 1: Mechanical properties

The relationship between the crack growth velocity and energy release rate in the reaction control regime is the following equation: $V = V_o e^{\left(\frac{Z\pi\sigma^2h}{4ENkT}\right)}$, where k is the Boltzmann constant, T the absolute temperature, N the bond density, and V_o a reference velocity. It shows that, under the same film stress, the crack growth velocity increases exponentially with film thickness h and constraint factor Z. Crack growth velocity is thus a sensitive measure of the effect of the substrate constraint on the energy release rate.

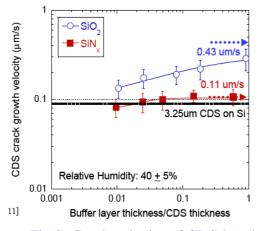


Fig.3: Crack velocity of CDS low-k film on top of a hard buffer layer

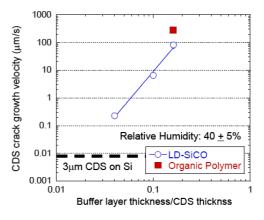


Fig.4: Crack velocity of CDS low-k film on top of a soft buffer layer.

Figure 3 shows the crack growth velocity of samples with hard buffer layers (SiO_2 , SiN_x .) The dash lines show the experimental results of CDS film on top of monolithic substrates. It shows that channeling cracks grow faster when CDS is deposited on buffer layers. The composition, bond structure, residual stress and elastic modulus of the CDS film do not depend on the buffer layer thickness. Consequently, the increased crack growth velocity can be attributed to the greater energy release rate (or lose of substrate constrain) as a result of inserting the SiN_x and SiO_2 buffer layers. As the buffer layer thickness increases, the channeling crack growth velocity increases and approaches limiting values indicated by the dash lines. The result of CDS on top of a 325nm thick SiN_x buffer layer is unexpected. It may result from either experimental control or channeling crack of SiN_x .

Figure 4 shows the crack growth velocity of samples with soft buffer layers (LD-SiCO, polymer.) The results show dramatic increase of crack velocity compared to a couple times of increase for samples with hard buffer layers. These observations show that: in addition to the residual stress, thickness, and fracture toughness of a coating, we also need to consider the precise film stack to determine whether the coating is prone to channel cracking.

The constraint factor Z depends on the Dundurs parameters for both interfaces as well as on the buffer layer thickness. This effect can be presented through use of an

"effective substrate modulus", which is calculated from experimental crack growth velocities. The effective substrate modulus is defined as the plane-strain modulus of a monolithic substrate that results in the same constraint factor as the system with the buffer layer. To deduce the effective substrate moduli, the crack velocity is first converted to the energy release rate according to the velocity-energy release rate curve (V-G curve) of a reference CDS sample with the same residual stress and thickness. Through eqn.1 and curve fitting of Beuth's numerical solution the effective substrate moduli are calculated and showed in Fig. 5 and Fig. 6:

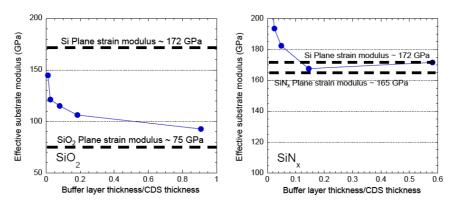


Fig.5: Effective substrate modulus of SiO₂/SiN_x buffer layer sample

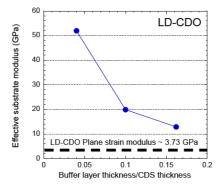


Fig.6: Effective substrate modulus of LD-CDO buffer layer sample

The above results show good evidence of lose of substrate constrain due to buffer

layers, especially for soft material like LD-CDO. The quantitative agreement is not good for thin SiN_x buffer layer. Probably the value of the effective modulus for a compliant film on a stiff substrate depends sensitively on the precise value of Dundurs parameter α .

Fig.7 shows the crack growth velocity of 3µm thick tensile CDS films on top of three different bi-layer systems: SiO₂/SiCN (180nm node), CDS/SiCN (90nm node) and LD-CDO/SiCN (45nm node). The data indicate that in a ten bi-layer structure, the channeling crack will be a significant issue for the integration of future 45nm technology node.

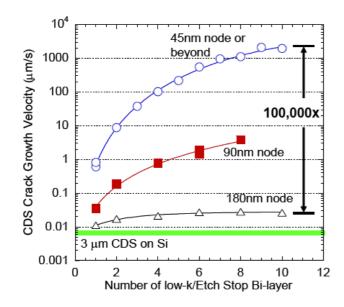


Fig.7: CDS crack velocity as a function of low-k/etch stop layers

Patterning effect

In a patterned Cu/low-k line structure, it is found that the energy release rate could be enhanced by the sample geometry at certain location. Fig.8 shows a patterned Cu/low-k line structure. Liu*3 built an elastic FEA model to evaluate the energy

release rate of low-k film in this patterned structure as a function of crack position, gap width w, Cu line thickness h_c , underlying low-k film thickness h_u , and the thickness h of low-k overlayer. The result shows that in the middle of the gap the energy release rate is largest. Fig.9 shows the relationship between gap width w and

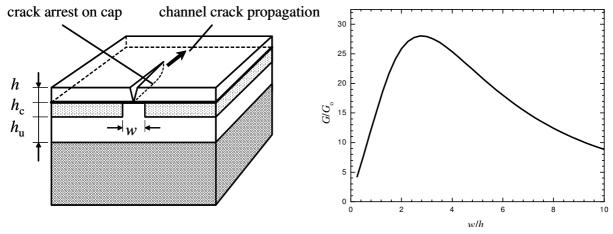
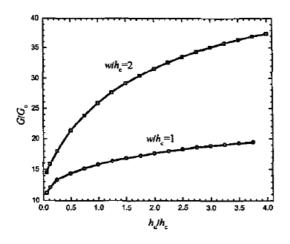


Fig.8: Multi-layer structure of underlying patterned metal and low-k dielectric layers with a channeling crack in the overlayer.

Fig.9: Energy release rate versus the gap width between metal pads.

the constrain factor Z of low-k film in the middle of the gap. In Liu's model, the energy release rate will reach a maximum when the ratio w/h_c approaches 2.75.

Fig. 10 shows the effect of increasing the thickness of underlying low-k films, while Fig. 11 shows the effect of increasing the thickness h of low-k film. The enhancement of constrain factor Z is due to the thermal mismatch and stiffness difference between the copper and low-k material, which in combination generate additional local stress in the overlayer. In this study, it is shown that the constrain factor Z can be enhanced to 35~40 due to Cu line structure.



35 30 25 20 15 10 0.0 0.5 1.0 1.5 2.0 2.5 3.0 hth_c

Fig.10: Effects of low-k underlayer thickness on the energy release rate.

Fig.11: Maximum energy release rate versus overlayer thickness.

Conclusion

The channeling crack growth of low-k film is demonstrated to be an important challenge in multilayer layer structure. The effective substrate modulus would be reduced by the underlying buffer layers and the low-k film is prone to cohesive failure. The substrate constrain factor might be further enhanced in patterned Cu/low-k line structure due to local stress concentration. Consequently, it is very important to consider the precise film stack to keep channeling crack from happening.

Reference

- 1. J.L. Beuth Jr., "Cracking of thin bonded films in residual tension", International Journal of Solids and Structures, 29, 1657-75 (1992)
- Ting Tsui et al., "Constraint Effects on Cohesive Failures in Low-k Dielectric Thin
 Films", Proceedings of the Materials Research Society 2005 spring meeting.
- 3. X. H. Liu, "Channel cracking in low-k films on patterned multi-layers", Proceedings of the IEEE 2004 International Interconnect Technology Conference, page 93-95.