Term paper for EM 397: Thin Film Mechanics

Fall 2006

Stress-Induced Voiding in Dual-Damascene Cu Interconnects

Abstract

Stress-induced voiding (SIV) is investigated in Cu-based, deep-submicron, dual damascene technology. Two failure modes are revealed by TEM failure analysis. For one mode, voids are formed under the via when the via connects a wide metal lead below it. For the via which is instead under a wide metal line, voids are formed right above the via bottom. The void source results from the supersaturated vacancies which develop when Cu is not properly annealed after electroplating and before being constrained by dielectrics. The driving force comes from the stress built up due to grain growth and the thermal expansion mismatch (CTE) between Cu interconnect and dielectrics. A diffusion model is introduced to investigate the voiding mechanism primarily for the vias connected to wide metal leads.

Introduction

Stress migration or stress induced voiding (SIV) is always one of the most important reliability concerns in both Al-based and Cu-based interconnects. Since SIV was first observed in Al interconnects in 1984, the issues surrounding Al-based SIV have been extensively investigated. Briefly, SIV is primarily a problem for narrow Al lines (< 4um) driven by the hydrostatic stress due to thermal mismatch between Al lines and its surrounding rigid dielectrics. For narrow Al lines with nearly bamboo grain structures, void firstly nucleates at grain boundary, then grows and finally produces open circuit. This problem is greatly mitigated by putting a redundant metal layer such as W underneath Al line to form a rigid two-layer structure. However, if the void occurs at the via, the resistance changes will be much larger and the problem is more complicated.

To meet the demand of high performance integrated circuits, Cu is used in current interconnects mainly due to its lower resistivity. Transition from Al-based to Cu-based interconnects requires the adoption of electro-chemical deposited (ECD) Cu processing and chemical mechanical polishing (CMP) techniques. In contrast to Al interconnects, whose reliability limitations has been well characterized for 30 years, Cu interconnect reliability is now being studied extensively. Since Cu has larger grain boundary activation energy, which results in a lower mobility, Cu is expected to have more resistance to SIV than Al under the same stress level. However, it seems that sometimes it is overly optimistic to assume that Cu has excellent SIV robustness, because Cu doesn’t have a natural oxide protection layer as Al and its SIV can be strongly process and structure dependent.

SIV Experiment

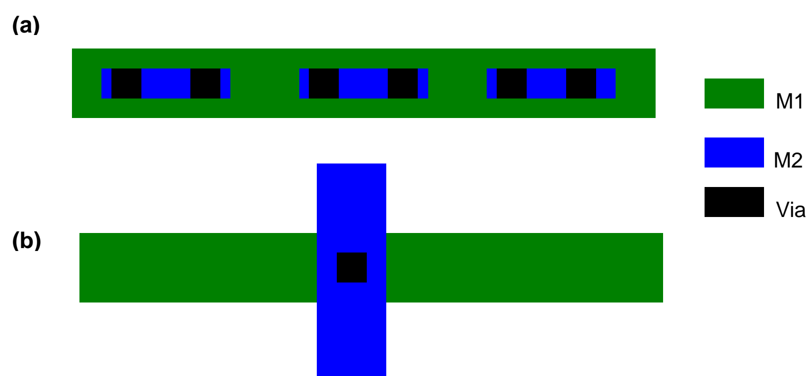

Fig. 1: Two typical test structures of SIV, (a) Via Chain (VC); (b) Van de Pauw (VDP)

Typically SIV can be experimentally characterized by using metal test structures that are sensitive to the SIV resistance rises. There are two typical test structures, as shown in Fig. 1. One is Van der Pauw (VDP) structure with a single via to easily trace the via resistance change and perform failure analysis using TEM or FIB; the other is the so called via chain (VC) structure with many vias connected through metal lines, for which the resistance rises of vias are magnified and easy to detect but it is relatively difficult to locate the failure loci. In the experiment, the test structures are stored in an unbiased conditions at elevated temperature (usually in the range of 150~200^{0}C). During baking the resistance rises are recorded at a certain interval. No current is applied to the test structure to eliminate the effect of electromigration-induced voiding.

Experimental observations of SIV in wide Cu lines

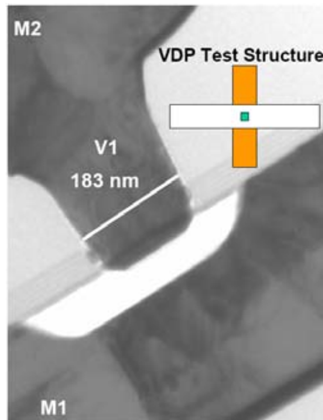

Fig. 2: Void-formation under a small via placed over a wide metal lead.

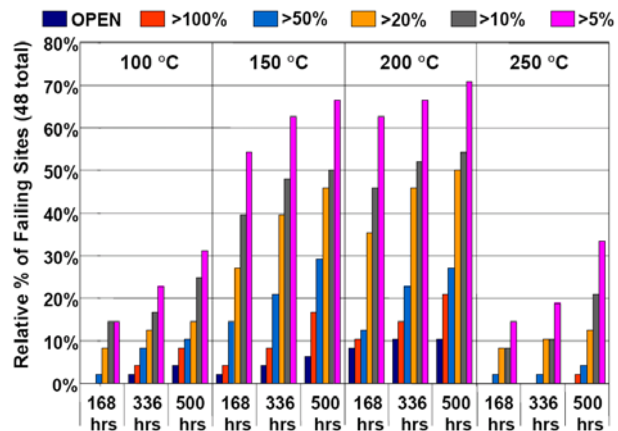

Fig. 3: Temperature-dependent resistance change data on VDP structures clearly showing stress-induced void phenomena.

Fig. 2 shows a TEM image of a VDP test structure with a narrow via sitting on a wider M1 lead. The void was formed after baking at 150^{0}C for over 100 hours. The Cu line was processed based on 180nm metallization technology using single damascene for M1 and dual-damascene for V1 and M2. Cu line was immediately planarized using CMP and encapsulated by nitride capping layer without post-ECD annealing. Since in the experiment, no bias was applied to the test structure, the observed resistance changes and subsequent failure should be a direct consequence of SIV. This interpretation can also be confirmed by comparing the failure rate at different temperatures. Fig. 3 is the temperature dependent failure rate of VDP structure. From the data set,

it is easily observed that voiding rate has a maximum value between 150^0C and 200^0C and fall off sharply above 200^0C, which is a strong indication of stress migration described by McPherson and Dunn's SM model.

The same experiment was also performed on the structure with narrow M1 line width (x10 narrower). It was found that no SIV was observed in the narrow structures, which seemed to be contradictory to the Al case where only "narrow" (~3um) Al lines have SIV problem.

Discussion

Active Diffusion Volume

During the baking process, two conditions are required to form the void: one is the vacancy source, the other is the driving force which drive the vacancy to the voiding position. The vacancies come from the grain growth at baking temperature. And the driving force is the tensile stress built up in the metal line. The tensile stress can be divided into two types according to its origin: thermal stress which is generated by the thermal expansion mismatch between the metal line and its surrounding dielectrics; and growth stress, which is induced by the grain growth within the metal lines. However, in the real test structure, only the vacancies within a certain region can diffuse and contribute to the void formation. From the mass transport point of view, it is very helpful to define the diffusion problem using three volumes. The first is defined by the geometry of metal lead, its length, width and height. The second is purely defined by the diffusion parameters, baking temperature and baking time. The third is the stress gradient region, which is where a significant tensile stress exists to compel vacancies to migrate to a specific voiding site. Voiding can only happen in the region where the above three volumes overlap, which is so-called coexistence region or "active diffusion volume". Using the concept of active diffusion volume, a lot of problems can be easily explained.

Line width dependence

As shown in Fig. 4, SIV is more severe in wider line structure because wider linewidth include larger active diffusion volume so that more vacancies can participate in the voiding process and the SIV is more significant.

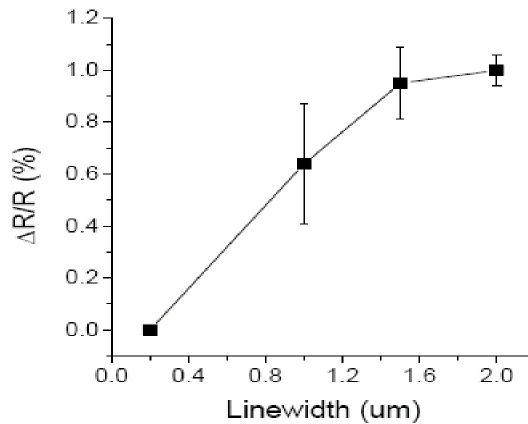

Fig. 4: Linewidth dependence of high temperature stress migration of Cu/FSG wide line structure with 190nm via.

Annealing Effect of Cu after ECD

Fig. 1 shows the void formed for Cu lines without post-ECD annealing. Then what happens if annealing is performed right after the ECD process and before capping layer deposition. Fig. 5 shows that post-ECD annealing can dramatically reduce the SIV failure rate and increase the Cu reliability. The reason is that ECD is a low temperature deposition process, and the as-deposited film has very small grain size. Grain will grow during post-ECD annealing and vacancies can diffuse to the free surface of the thin film so that in the later high temperature storage experiment, not much grain growth can happen and both the vacancy source and driving force can be significantly reduced.

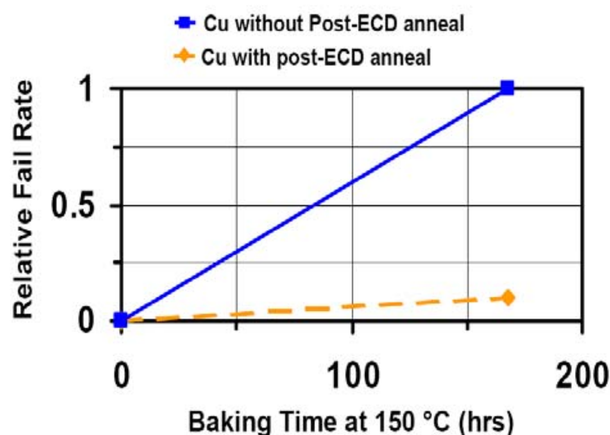

Fig. 5: Bake failure rate comparison for Cu with post-ECD annealing Cu without post-ECD annealing.

Advanced Issues

All the above experiment and discussion are based on the structure in which a small via

overlies on a wide M1 line. Void is observed to grow right under the via. However, void can also grow within the via if the via is placed under a wide M2 line, as shown in Fig. 6. This kind of voiding can be eliminated if the via shape is properly engineered. Experiments are also performed to investigate the interface engineering effect. If the nitride capping layer is replaced by a redundant metal layer such as W or CoWB, the line width dependence of SIV can be also be eliminated, which indicates that interface is really a fast diffusion path and SIV of Cu interconnects are very process dependant. The incorporation of low-k materials has both positive and negative effects in SIV reliability. On the one hand, low-k materials have larger thermal expansion coefficient, which is closer to the CTE of Cu and makes the thermal mismatch between them smaller and the tensile stress smaller; one the other hand, low-k materials have weaker mechanical properties than oxide, which makes low-k materials more susceptible to defects and easier to voiding.

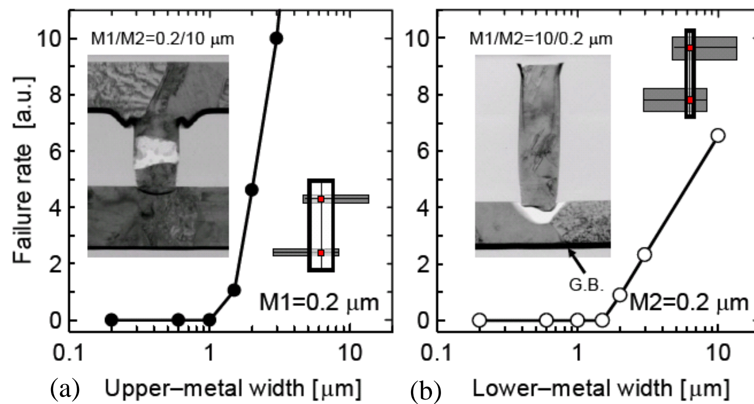

Fig. 6: Two failure modes revealed by TEM; (a) Upper-metal mode with wide M2 above small via, (b) Lower-metal mode with wide M1 under small via.

Summary

Stress-induced voiding occurs and is most severe at vias connected to wide Cu metal leads. Active diffusion volume, which is a region where interconnect geometry, diffusion mechanism and stress gradient region coexists, can successfully explain a lot of phenomena such as SIV difference between Cu lines with and without post-ECD annealing, and line width dependence. Two modes of SIV are observed in experiment, and the so-called upper-metal mode can be eliminated by via shape engineering. During voiding process, the vacancy source comes from the grain growth, and the required tensile stress comes from thermal expansion mismatch and grain growth. Interface and grain boundary are two fast diffusion paths. By replacing nitride capping

layer by a redundant metal layer such as W, the line width dependence of SIV can be eliminated. It indicates that SIV in Cu interconnects are very much process dependent.

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